Advait Paranjpe

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Education

University of California, Los Angeles (UCLA), M.S. in Electrical and Computer Engineering *Sep 2025 – Jul 2027*

- Specializing in computer architecture, digital IC design, and FPGA/RTL development**.**

The University of Manchester (UoM), B.Eng. in Electrical and Electronic Engineering *Sep 2022 – Jul 2025*

- Final Score: First Class Honours (Top Classification; ~4.0/4.0 Equiv).
- Dissertation: "Cascaded PLL Microwave Synthesizer for 5G systems".

Experience

National Energy System Operator | Backend Software Engineering Intern *Jul 2025 – Sep 2025*

- Refactored a critical 100k+ LOC tool with vectorization, delivering a 10x faster daily run, saving 450+ hours annually.
- Achieved 60x faster price-forecasting runs by building a Bayesian decision engine, informing stakeholders of investment risks.
- Delivered a 24x faster simulation-input pipeline by parallelizing and batching API requests, improving cost-forecast fidelity.
- Processed 100M+ rows via chunked parallelization, cutting RAM usage from 32 to 16 GB, achieving 11x faster execution time.

National Grid ESO | Data Engineering Intern *Jul 2024 – Sep 2024*

- Integrated the Elexon API into a Python service to maintain up-to-date bid/offer values, saving 400+ manual hours annually.
- Designed an electrical grid data processing pipeline, using Pandas and NumPy, increasing parsing efficiency by 40%.
- Translated 100M+ data points into intuitive, stakeholder-friendly formats, enabling faster model reviews and clearer decisions.

BMW | Electronics and Systems Technology Intern *Jul 2019 – Aug 2019*

- Helped build C++ tooling for the MGU22 infotainment platform for regenerative-braking diagnostics, shortening test cycles.

Projects

PixelForge | FPGA Retro Graphics Engine (Basys3/Artix-7) *Jan 2026 – Feb 2026*

- Built an FPGA retro graphics engine (sprite + tilemap renderer) and demoed real-time VGA output on Basys3.
- Implemented SV VGA timing + pipelined pixel path (640*480@60); closed post-route timing (WNS +1.3 ns @100 MHz).
- Developed BRAM-backed tile/sprite compositor; ~2.1k LUT / 2.6k FF / 8 BRAM, Fmax ~165 MHz.
- Created self-checking SV testbench + SVA (~120 asserts) and did on-board debug with ILA, fixing 6 corner bugs pre-bitstream.

SpeakUp | Real-Time Sign Language to Speech Translator *(Python and C)* *Mar 2025 – Apr 2025*

- Built an embedded ASL to speech translator on Raspberry Pi 3 + Sony IMX500 for fully offline use.
- Achieved real-time on-device inference (~18 fps) with ~180 ms end-to-end latency on resource-constrained hardware.
- Fine-tuned & quantized MobileNetV2 (TensorFlow) for gesture recognition, achieving ~91% accuracy.
- Integrated recognition with eSpeak TTS, producing speech with ~250 ms time-to-first audio and ~120 ms audio lag.
- Optimized capture to NN to TTS with pipelining & thread pinning, holding CPU <70%, RAM <220 MB and power <=3.2 W.

Dissertation | Novel Tunable Microwave Frequency Synthesizer *(Python, C++ and C)* *Sep 2024 – Mar 2025*

- Architected a 5G synthesizer with a novel cascaded-PLL topology, achieving sub -150 dBc/Hz at 10kHz offset at 15 GHz.
- Validated novel design using a spectrum analyzer, outperforming Texas Instruments eval-board limits by 20 dBc/Hz.
- Specified a register map and CRC-protected SPI protocol with read-back verification, providing an RTL/FPGA-ready interface.
- Delivered first-pass signal integrity on a high-speed RF board by enforcing controlled impedance and robust PDN decoupling.
- Implemented C/C++ firmware and a Python GUI to achieve switching under 1 second and 3× faster frequency calibration.

STMicroelectronics | Autonomous Line Tracking Buggy *(C++)* *Oct 2023 – May 2024*

- Developed a PID controller, achieving 100% line-tracking accuracy, leading to a top 3 finish among 50+ teams.

Skills

- **Languages:** Python, C/C++, JavaScript, SQL, MATLAB
- **HDL/RTL:** SystemVerilog, VHDL/Verilog | Vivado, XDC | SVA (assertions), ILA (debug)
- **Software/Tools:** NumPy, Pandas, PostgreSQL, Docker, Git, CI/CD; REST APIs; async/multiprocessing
- **Embedded/EDA:** SPI/I²C/UART, TCP/UDP/IP, CRC/read-back; Altium, LTspice, Simulink